CLAIMS

What is claimed is.

1. A method of forming a device comprising:

patterning a first oxide upon a substrate;

forming a first nitride spacer mask upon the first oxide;

forming a first oxide spacer mask upon the first nitride spacer mask;

forming a second nitride spacer mask upon the first oxide spacer mask;

forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask; and

forming a gate layer over the plurality of channels, wherein each of the plurality of channels is narrower than the mean free path of semiconductive electron flow therein.

2. The method according to claim 1, wherein forming a first nitride spacer mask comprises:

forming a first nitride layer over the first oxide; and

performing a reactive ion etch upon the first nitride layer.

3. The method according to claim 1, wherein forming a first oxide spacer mask upon the first nitride spacer mask comprises:

forming a first oxide layer over the first nitride spacer mask; and

performing a reactive ion etch upon the first oxide layer.

4. The method according to claim 1, wherein forming a second nitride spacer mask upon the first oxide spacer mask comprises:

forming a second nitride layer over the first oxide spacer mask: and

performing a reactive ion etch upon the second nitride layer.

5. The method according to claim 1, wherein forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask comprises:

performing a gate etch with the second nitride spacer masks.

6. The method according to claim 1, wherein forming a first nitride spacer mask comprises:

forming a first nitride layer over the first oxide; and

performing a reactive ion etch upon the first nitride layer, wherein forming a first oxide spacer mask upon the first nitride spacer mask comprises:

forming a first oxide layer over the first nitride spacer mask; and

performing a reactive ion etch upon the first oxide layer, wherein forming a second nitride spacer mask upon the first oxide spacer mask comprises:

forming a second nitride layer over the first oxide spacer mask; and

performing a reactive ion etch upon the second nitride layer, wherein forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask comprises:

performing a gate etch with the second nitride spacer masks, and further comprising: forming a gate oxide upon the plurality of channels.

7. The method according to claim 1, wherein the first oxide is patterned with a width of about 100 nm and a pitch of about 300 nm.

8. The method according to claim 1, wherein the first oxide is patterned with a width of about 100 nm and a pitch of about 320 nm.

9. The method according to claim 1, wherein the substrate is made by providing a silicon on insulator substrate, and wherein the plurality of channels comprises monocrystalline silicon channels.

10. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, and wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels.

11. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, and wherein a doping region is disposed in the substrate beneath the trench that resists electrical communication between adjacent spaced-apart channels.

12. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein the trench is filled with a dielectric, and wherein

the plurality of channels comprises a plurality of single-gate quantum wire field effect transistors.

13. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein each of the plurality of channels has a gate oxide layer disposed thereupon, and wherein the second nitride spacer mask is disposed between the channel and the gate layer.

14. The method according to claim 1, wherein the plurality of channels comprises a plurality of triple-gate quantum wire field effect transistors.

15. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein a doping region is disposed in the substrate beneath the trench that resists electrical communication between adjacent spaced-apart channels, and wherein the substrate is part of a silicon on insulator structure.

16. A method of forming a device comprising:

patterning a first oxide having a first width upon a substrate;

forming a first nitride layer upon the first oxide and the substrate, wherein the first nitride layer has a first thickness that is less than the first width;

forming a first nitride spacer mask from the first nitride layer, wherein the first nitride spacer mask has a width equal to the first nitride layer thickness;

forming an oxide layer upon the first nitride spacer mask, wherein the oxide layer has a second thickness that is less than the width of the first nitride spacer mask;

forming a first oxide spacer mask from the oxide layer, wherein the first oxide spacer mask has a width equal to the first oxide layer thickness;

forming a second nitride layer upon the first oxide spacer mask, wherein the second nitride layer has a thickness that is less than the width of the first oxide spacer mask;

forming a second nitride spacer mask from the second nitride layer;

removing the first oxide spacer mask;

performing an etch over the second nitride spacer mask to form at least one semiconductor channel having a channel width and a length, wherein the mean free electron path therein is larger than the channel width;

forming a dielectric layer upon the channel length; and

forming a gate layer over the channel.

17. The method according to claim 16, wherein the first oxide has a width of X and a pitch of about 3X.

18. The method according to claim 16, wherein each performing a spacer etch comprises performing a reactive ion etch.

19. The method according to claim 16, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels, wherein each of the plurality of semiconductive channels has a width of about one-tenth X;

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

20. The method according to claim 16, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

removing the patterned second nitride spacer mask;

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

21. The method according to claim 16, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

forming an oxide upon the SOI topology;

forming a gate layer over the oxide; and

forming a contact that connects with the plurality of channels, wherein the contact has a characteristic width from about 2X to about 10X.

22. A method of forming a device comprising:

patterning a first oxide upon a substrate, wherein the first oxide has a characteristic width of X and a characteristic pitch selected from about 3X and about 3.2X:

forming a first nitride layer upon the oxide, wherein the first nitride layer has a characteristic thickness of about one half X;

performing a spacer etch upon the nitride layer and removing the oxide to form a patterned first nitride spacer mask;

forming an oxide layer upon the patterned first nitride spacer mask, wherein the oxide layer has a characteristic thickness of about one fourth X;

performing a spacer etch upon the oxide layer and removing the patterned first nitride spacer mask to form a patterned first oxide spacer mask;

forming a second nitride layer upon the patterned first oxide spacer mask, wherein the second nitride layer has a characteristic thickness of about one-tenth X; and

performing a spacer etch upon the second nitride layer and removing the first oxide spacer mask to form a patterned second nitride spacer mask.

23. The method according to claim 22, further comprising:

performing an etch over the patterned second nitride spacer mask to form at least one semiconductor channel wherein the mean free electron path therein is larger than about one-tenth X.

24. The method according to claim 22, wherein X is in a range from about 20 nm to about 200 nm.

25. The method according to claim 22, wherein each performing a spacer etch comprises performing an reactive ion etch.

26. The method according to claim 22, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

27. The method according to claim 22, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

removing the patterned second nitride spacer mask;

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

28. The method according to claim 22, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

forming an oxide upon the SOI topology;

forming a gate layer over the oxide; and

forming a contact that connects with the plurality of channels, wherein the contact has a characteristic width from about 2X to about 10X.

29. A device comprising:

a plurality of semiconductive channels, each of the plurality of semiconductive channels comprising a channel length and a channel width;

a dielectric layer disposed upon the semiconductive channel length;

a source at a first terminal end of the plurality of semiconductive channels. and a second terminal end of the plurality of semiconductive channels;

a gate layer disposed over the dielectric layer, wherein electron flow in the plurality of semiconductive channels has a mean free path that is greater than the semiconductive channel width, and wherein a first semiconductive channel is spaced apart from a second semiconductive channel by a trench that is less than about five times the semiconductive channel width.

30. The device according to claim 29, wherein the plurality of semiconductive channels comprises monocrystalline silicon that is disposed upon a dielectric.

31. The device according to claim 29, wherein the plurality of semiconductive channels comprises monocrystalline silicon that has a self-aligned doping region in the monocrystalline silicon beneath the trench.

32. The device according to claim 29, further comprising:

a mask disposed upon the semiconductive channel width, wherein the device comprises a double-gate quantum wire.

33. The device according to claim 29, wherein the semiconductive channel width is in a range from less than or equal to about 5 nm to about 30 nm.

34. The device according to claim 29, further comprising:

a mask disposed upon the semiconductive channel width, wherein the trench is filled with material comprising the gate layer.

35. The device according to claim 29, wherein the device comprises a triple-gate quantum wire.

36. The device according to claim 29, further comprising:

a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels upon a contact landing pad.

37. The device according to claim 29, further comprising:

a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact has a characteristic width in a range from about 200 nm to about 1,000 nm.

38. The device according to claim 29, further comprising:

a trench disposed between the first semiconductive channel and the spaced-apart second semiconductive channel, wherein the trench is filled with the dielectric material that is disposed on the semiconductive channel length.

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